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Product Code WM-G-MR-05
Product No.

Product Specification
of
WM-G-MR-05

Wireless LAN Module

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1 REVISION HISTORY

Version No.	Revised Date	Revised by	Description	Notes
1.0	2006-02-16	Jaddy Chen	Preliminary specification released	
1.1	2006/10/23	Jaddy Chen	Update power consumption data Sec. 5.1 Add Vdd_PA Sec.6.1 update pin definition pin12 Sec.8 Modify module drawing	
1.2	2006/11/02	Jaddy Chen	Update Radio Specification Sec. 5.2 Recommend Operating Condition Sec. 5.5 Tx & Rx Performance	
1.3	2006/11/09	Jaddy Chen	Modify Recommend Footprint (Sec. 9)	
1.4	2007/1/24	Jaddy Chen	Add Laser Mark on the shielding	
1.5	2007/3/19	Jaddy Chen	Add Package and storage condition	
1.6	2007/4/17	Jaddy Chen	Add EVM Spec (Page 8,9)	
1.7	2007/4/24	Jaddy Chen	Update Power Consumption	
1.8	2008/02/21	Jaddy Chen	Update Regulatory Test	

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2 **PURPOSE**

The purpose of this document is to define the product specification for 802.11b/g WiFi module WM-G-MR-05.

3 **SCOPE**

- High speed for wireless LAN connection: IEEE802.11b/g up to 54Mbps data rate by incorporating Direct Sequence Spread Spectrum (DSSS) and OFDM data modulation.
- Provide seamless roaming within the IEEE 802.11b/g WLAN infrastructure.
- IEEE 802.11b/g compatible: allow inter-operation among multiple vendors.
- Auto fallback: 54M, 48M, 36M, 24M, 18M, 12M, 9M, 6M (802.11g); 11M, 5.5M, 2M, 1M (802.11b) data rate with auto fallback.
- WPA (Wi-Fi Protected Access)
- Support 802.11i Security standard through implementation of AES / CCMP and WEP with TKIP security mechanism.
- Support 802.11e Quality of Service (QoS)
- Interoperability – Complying with WECA WiFi.
- 3-wire, hardware signaling BT WiFi co-existence supported

4 GENERAL FEATURES

	Item	Description	Notes
802.11b/g	Standard	Complies with the latest IEEE802.11b/g wireless LAN Physical Layer Specification (IEEE 802.11g dated 12/6/2003)	
	Chip Set	Marvell 88W8686	
	Module Interface Type	SDIO (1bit and 4 bit) , SDIO_SPI , G-SPI	
	Module Connection	48pin LGA	
	Co-existence	Supports 3-wire BT coexistence scheme for an external BT solution	
	Data Rate	802.11g: 54, 48, 36, 24, 18, 12, 9, 6 Mbps, auto rate 802.11b: 11, 5.5, 2, 1Mbps, auto rate	
	Modulation	OFDM (54, 48, 36, 24, 18, 12, 9, 6Mbps) CCK (11Mbps, 5.5Mbps) DQPSK (2Mbps) DBPSK (1Mbps)	
	Operating Frequency	2.4GHz ISM band	
	Operating Channels	IEEE Channels 1–14 depending on Regulatory Domain settings	
	Others	Compliance with FCC Class B Part 15.247, R&TTE, TELEC major RF regulatory requirements	

5 ELECTRICAL SPECIFICATION

5.1 SUPPLY VOLTAGE

Symbol	Parameter	Min	Typ	Max	Unit
VDD18A	1.8V Analog power supply	1.7	1.8	1.9	V
VDD18_LDO	Internal 1.2V LDO, BT COEX	1.62	1.8	1.98	V
VDD30	TR SW, ANT SW, PA_PE	2.7	3.0	3.3	V
VDD_PA	PA Power Supply	3.0	3.3	3.6	
VDD_SHI	Host IF, GPIO, RESETn, CLK_OUT, TMS2	1.62	1.8	1.98	V
		2.97	3.3	3.63	V
VIO_X2	EEPROM, JTAG	1.62	1.8	1.98	V
		2.97	3.3	3.63	V

5.2 RECOMMENDED OPERATION CONDITIONS

5.2.1 TEMPERATURE, HUMIDITY

Symbol	Parameter	Min	Typ	Max	Unit
TA	Ambient Operation Temperature	-10	-	65	⁰ C
Humidity	Relative Humidity			95	%

Symbol	Parameter	Min	Typ	Max	Units
VDD1.8	Power supply voltage with respect to GND	1.7	1.8	1.9	V
VDDA	Power supply voltage with respect to GND	2.7	3.0	3.3	V
VDD_SHI	Power supply voltage with respect to GND	1.62	1.8	1.98	V
		2.97	3.3	3.63	
VIO_X2	Power supply voltage with respect to GND	2.97	3.3	3.63	V
VDD_PA	Power supply voltage with respect to GND	3.0	3.3	3.6	V

5.2.2 (SDIO/SPI/JTAG/RESET/COEXISTENCE/GPIO)

DC Electricals.1.8V/3.3V (VDD_SHI/VIO_X2) (VIO_X2 not support 1.8V Mode)

Symbol	Parameter	Operating Mode	Condition	Min	Typ	Max	Units
V18	Power supply voltage	1.8V	--	1.62	1.8	1.98	V
V33	Power supply voltage	3.3V	--	2.97	3.3	3.63	V
VIH	Input high voltage	1.8V	--	1.2	--	V18+0.3	V
		3.3V	--	2.0	--	V33+0.3	V
VIL	Input low voltage	1.8V	--	-0.3	--	0.6	V
		3.3V	--	-0.3	--	1	V
VHYS	Input hysteresis	1.8V	--	250	--	--	mV
		3.3V	--	300	--	--	mV

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VOH	Output high voltage	1.8V	--	1.22	--	--	V
		3.3V	--	2.57	--	--	V
VOL	Output low voltage	1.8V	--	--	--	0.4	V
		3.3V	--	--	--	0.4	V
IOH @ 1.62V-0.4V	Output high current	1.8V	SR[1:0]=3	7.5	12	16	mA
IOL @ 0.4V	Output low current	1.8V	SR[1:0]=3	8	16.5	23	mA
IOH @ 1.62V-0.6V	Output high current	1.8V	SR[1:0]=3	10	16	22	mA
IOL @ 0.6V	Output low current	1.8V	SR[1:0]=3	10	22	32	mA
IOH @ 1.62V-0.4V	Output high current	1.8V	SR[1:0]=2	7.5	12	16	mA
IOL @ 0.4V	Output low current	1.8V	SR[1:0]=2	5	11	15.5	mA
IOH @ 1.62V-0.6V	Output high current	1.8V	SR[1:0]=2	10	16	22	mA
IOL @ 0.6V	Output low current	1.8V	SR[1:0]=2	6.5	14.5	21	mA
IOH @ 1.62V-0.4V	Output high current	1.8V	SR[1:0]=1	2.5	4	5	mA
IOL @ 0.4V	Output low current	1.8V	SR[1:0]=1	2.5	5.5	7.5	mA
IOH @ 1.62V-0.6V	Output high current	1.8V	SR[1:0]=1	3	5	7	mA
IOL @ 0.6V	Output low current	1.8V	SR[1:0]=1	3	7	10.5	mA
IOH @ 1.62V-0.4V	Output high current	1.8V	SR[1:0]=0	2.5	4	5	mA
IOL @ 0.4V	Output low current	1.8V	SR[1:0]=0	2.5	5.5	7.5	mA
IOH @ 1.62V-0.6V	Output high current	1.8V	SR[1:0]=0	3	5	7	mA
IOL @ 0.6V	Output low current	1.8V	SR[1:0]=0	3	7	10.5	mA
IOH @ 2.97V-0.4V	Output high current	3.3V	SR[1:0]=3	9.5	13.5	16.5	mA
IOL @ 0.4V	Output low current	3.3V	SR[1:0]=3	10	18	23.5	mA
IOH @ 2.97V-0.6V	Output high current	3.3V	SR[1:0]=3	13	18.5	23	mA
IOL @ 0.6V	Output low current	3.3V	SR[1:0]=3	13.5	24.5	33	mA
IOH @ 2.97V-0.4V	Output high current	3.3V	SR[1:0]=2	9.5	13.5	16.5	mA
IOL @ 0.4V	Output low current	3.3V	SR[1:0]=2	6.5	12	15.5	mA
IOH @ 2.97V-0.6V	Output high current	3.3V	SR[1:0]=2	13	18.5	23	mA
IOL @ 0.6V	Output low current	3.3V	SR[1:0]=2	9	16	22	mA
IOH @ 2.97V-0.4V	Output high current	3.3V	SR[1:0]=1	3	4.5	5.5	mA
IOL @ 0.4V	Output low current	3.3V	SR[1:0]=1	3	6	7.5	mA
IOH @ 2.97V-0.6V	Output high current	3.3V	SR[1:0]=1	4	6	7.5	mA
IOL @ 0.6V	Output low current	3.3V	SR[1:0]=1	4.5	8	10.5	mA
IOH @ 2.97V-0.4V	Output high current	3.3V	SR[1:0]=0	3	4.5	5.5	mA
IOL @ 0.4V	Output low current	3.3V	SR[1:0]=0	3	6	7.5	mA
IOH @ 2.97V-0.6V	Output high current	3.3V	SR[1:0]=0	4	6	7.5	mA
IOL @ 0.6V	Output low current	3.3V	SR[1:0]=0	4.5	8	10.5	mA
I_pullup	--	--	--	15.7	21.7	28.7	μA
I_pulldown	--	--	--	11.8	22.5	33.1	μA
I_pullup_weak	--	--	--	2.1	2.4	3.4	μA
I_pulldown_weak	--	--	--	1.3	3	4.9	μA

5.2.3 AC ELECTRICAL

Symbol	Parameter	Operating Mode	Condition	Min	Typ	Max	Units
T _{SLEW_RISE} @ 10 pF Load	Output rise slew rate when SR[1:0] = 3	1.8V	0.2*V18 - 0.8*V18	0.58	1.05	1.65	V/ns
		3.3V	0.2*V33 - 0.8*V33	0.81	1.39	2.08	V/ns
T _{SLEW_FALL} @ 10 pF Load	Output fall slew rate when SR[1:0] = 3	1.8V	0.8*V18 - 0.2*V18	0.6	1.34	2.38	V/ns
		3.3V	0.8*V33 - 0.2*V33	0.73	1.49	2.21	V/ns
T _{SLEW_RISE} @ 10 pF Load	Output rise slew rate when SR[1:0] = 2	1.8V	0.2*V18 - 0.8*V18	0.58	1.05	1.65	V/ns
		3.3V	0.2*V33 - 0.8*V33	0.81	1.39	2.08	V/ns
T _{SLEW_FALL} @ 10 pF Load	Output fall slew rate when SR[1:0] = 2	1.8V	0.8*V18 - 0.2*V18	0.4	0.88	1.38	V/ns
		3.3V	0.8*V33 - 0.2*V33	0.64	1.29	1.86	V/ns
T _{SLEW_RISE} @ 10 pF Load	Output rise slew rate when SR[1:0] = 1	1.8V	0.2*V18 - 0.8*V18	0.19	0.34	0.5	V/ns
		3.3V	0.2*V33 - 0.8*V33	0.38	0.59	0.82	V/ns
T _{SLEW_FALL} @ 10 pF Load	Output fall slew rate when SR[1:0] = 1	1.8V	0.8*V18 - 0.2*V18	0.2	0.45	0.68	V/ns
		3.3V	0.8*V33 - 0.2*V33	0.36	0.7	0.89	V/ns
T _{SLEW_RISE} @ 10 pF Load	Output rise slew rate when SR[1:0] = 0	1.8V	0.2*V18 - 0.8*V18	0.19	0.34	0.5	V/ns
		3.3V	0.2*V33 - 0.8*V33	0.38	0.59	0.82	V/ns
T _{SLEW_FALL} @ 10 pF Load	Output fall slew rate when SR[1:0] = 0	1.8V	0.8*V18 - 0.2*V18	0.2	0.45	0.68	V/ns
		3.3V	0.8*V33 - 0.2*V33	0.36	0.7	0.89	V/ns

5.3 POWER CONSUMPTION (SDIO MODE)

The power consumption is typical value measured at 25°C temperature

Voltage : VDD3.3 (VDD3.0, VDD_SHI, VIO_X2 and VDD_PA)

Operating Voltage	3.0~3.6 Volt	
Current		
Condition	Typical (3.3V, 25 degree C)	Maximum (3.3V, 25 degree C)
Transmit(54Mbps, 12 dBm)	125mA	160mA
Transmit(11Mbps, 14 dBm)	135mA	165mA
Receive(54Mbps, -70 dBm)	1mA	3mA
Receive(11Mbps, -70 dBm)	1mA	3mA
Deep Sleep (Use Labtool command 26 1)	0.3mA	0.5mA

Voltage : VDD1.8 & OSCILLATOR

Operating Voltage	1.7 ~ 1.9 Volt	
Current		
Condition	Typical (1.8V, 25 degree C)	Maximum (1.8V, 25 degree C)
Transmit(54Mbps, 12 dBm)	140mA	160mA
Transmit(11Mbps, 14 dBm)	130mA	150mA
Receive(54Mbps, -70 dBm)	170mA	180mA
Receive(11Mbps, -70 dBm)	150mA	160mA
Deep Sleep (Use Labtool command 26 1)	0.26mA	0.4mA

5.4 WIRELESS SPECIFICATIONS

The WM-G-MR-05 module complies with the following features and standards:

Features	Description
WLAN Standards	IEEE 802 Part 11b/g (802.11b/g)
Antenna Port	One antenna port support 802.11b/g
Coexistence	Hardware signaling
Frequency Band	2.400 – 2.484 GHz

5.5 RADIO SPECIFICATIONS

Over full range of values specified in the “Recommended Operation Condition” unless specified otherwise.

Features	Description
Frequency Band	2.4000 – 2.497 GHz (2.4 GHz ISM Band)
Number of selectable Sub channels	14 channels
Modulation	OFDM, DSSS (Direct Sequence Spread Spectrum), DBPSK, DQPSK, CCK , 16QAM, 64QAM
Supported rates	1, 2, 5.5, 11, 6, 9, 12, 18, 24, 36, 48, 54 Mbps
Maximum receive level	- 10dBm (with PER < 8%)
Output Power	14 dBm +2.0 /-1.5 dBm for 1, 2, 5.5, 11Mbps 12 dBm +2.0 /-1.5 dBm for 6 , 9 and > 12Mbps

802.11g EVM Requirement

Item	Data Rate (Mbps)	Relative Constellation Error (dB)	EVM (%RMS)
1	6 (BPSK)	-5	56.2
2	9 (BPSK)	-8	39.8
3	12 (QPSK)	-10	31.6
4	18 (QPSK)	-13	22.4
5	24 (16-QAM)	-16	15.8
6	36 (16-QAM)	-19	11.2
7	48 (64-QAM)	-22	7.9
8	54 (64-QAM)	-25	5.6

802.11b EVM

Item	Data Rate (Mbps)	EVM (%RMS)
1	1 (BPSK)	35%
2	2 (QPSK)	35%
3	5.5 (QPSK)	35%
4	11 (QPSK)	35%

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Sensitivity

Receiver Characteristics (3.3V, 25 degree C)	Typical	Maximum	Unit
PER <8%, Rx Sensitivity @ 11 Mbps	-87	-85	dBm
PER <8%, Rx Sensitivity @ 1 Mbps	-93	-91	dBm
PER <10% Rx Sensitivity @ 6 Mbps	-86	-84	dBm
PER <10%, Rx Sensitivity @ 54 Mbps	-72	-70	dBm

6 INTERFACE

6.1 PIN DEFINITION

No.	Definition	Type	Draft Description	Power Domain
1	GND	Ground	Ground	Ground
2	RF_OUT	I/O	RF port for antenna or RF connector	-
3	GND	Ground	Ground	Ground
4	NC	NC	No Connect Do not connect this pin. Leave it floating.	-
5	JTAG_TCK	I	Internal 100 kΩ pull-up JTAG Test Clock.	VIO_X2
6	JTAG_TDO	O	JTAG Test Data Output	VIO_X2
7	JTAG_TMS_ARM	I	Internal 100 kΩ pull-up JTAG Test Mode Select 2 This input selects the ARM JTAG controller.	VIO_X2
8	NC	NC	No Connect Do not connect this pin. Leave it floating.	-
9	JTAG_TRSTn	I	Internal 100 kΩ pull-up JTAG Test Reset, active low.	VIO_X2
10	JTAG_TDI	I	Internal 100 kΩ pull-up JTAG Test Data Input	VIO_X2
11	GPIO_6	I/O	Internal pull-up General Purpose Input/Output	VDD_SHI
12	VDD_30	Power	I/O Analog Power Supply	VDDA_30
13	GND	Ground	Ground	Ground
14	GPIO_1	I/O	WLAN LED control signal, drive the LED indicating the link status of WLAN. Active low.	VDD_SHI
15	GPIO_2	I/O	Internal pull-up General Purpose Input/Output	VDD_SHI
16	GPIO_4 / Host Wake-up	I/O	Internal pull-up 1) General Purpose Input/Output 2) WLAN MAC wake-up in / interrupt in	VDD_SHI
17	GPIO_0 / REFCLK_EN	O	REF_CLK source enable pin. During power down sleep mode, if implemented, external oscillator is also powered down by this control.	VDD_SHI
18	GND	Ground	Ground	Ground
19	REF_CLK	I	External clock source: 19.2, 20, 26, 38.4, 40 ,44MHz, selected by internal resistor configuration.	VDD1.8 in DC coupled mode
20	GND	Ground	Ground	Ground
21	PDn	I	Internal pull-up	VDD_SHI

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			Full Power Down (active low)	
22	SLEEP_CLK	I	External sleep clock input	VDD_SHI
23	G-SPI_RSTn	I	Internal 100 kΩ pull-up. Reset Pin, active low.	VDD_SHI
24	VDD_SHI	Power	Digital I/O power supply	VDD_SHI
25	GND	Ground	Ground	Ground
26	GND	Ground	Ground	Ground
27	RESETn	I	Internal 100 kΩ pull-up. Module reset - active low	VDD_SHI
28	NC	NC	No Connect Do not connect this pin. Leave it floating.	-
29	NC	NC	No Connect Do not connect this pin. Leave it floating.	-
30	GND	Ground	Ground	Ground
31	GND	Ground	Ground	Ground
32	VIO_X2	Power	3.3V Digital Power Supply	VIO_X2
33	WLAN_ACTIVE	I/O	<p>WLAN Active (active low)</p> <p>2-Wire BCA Mode: When high, WLAN is transmitting or receiving packets.</p> <p>3-Wire BCA Mode: 0 = Bluetooth device allowed to transmit 1 = Bluetooth device not allowed to transmit</p> <p>Internal 50 k pull-down. This pin drives low when PDn is asserted. In WLAN Sleep mode, all I/O PADs are powered down. This Pad must stay at a low state even in power down mode.</p> <p>NOTE: In 3WBCA mode, WL_ACTIVEn output is programmable and can be 0 during both BT Rx and BT Tx timeslots.</p>	VDD1.8
34	BT_PRIORITY	I/O	<p>Bluetooth Priority</p> <p>2-Wire BCA Mode: When high, BT is transmitting or receiving high priority packets.</p> <p>3-Wire BCA Mode: When high, BT is transmitting or receiving packets.</p>	VDD1.8
35	BT_STATE	I/O	<p>Bluetooth State</p> <p>0 = normal priority, Rx 1 = high priority, Tx</p>	VDD1.8

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			Priority is signaled after BT_PRIORITY has been asserted. After priority signaling, BT_STATE indicates the Tx/Rx mode of BT radio.	
36	PA_GND1	Ground	GND for RF power amplifier	Ground
37	PA_GND	Ground	GND for RF power amplifier	Ground
38	VDD_PA1	Power	3.3V Power supply for PA	VDD_PA
39	VDD_PA	Power	3.3V Power supply for PA	VDD_PA
40	SDIO_D3	I/O	SDIO 4-bit Mode: Data Line Bit[3] SDIO 1-bit Mode: Reserved SDIO SPI Mode: Card Select (active low)	VDD_SHI
41	SDIO_D2	I/O	G-SPI mode : G-SPI Interrupt Output (active low) SDIO mode : SDIO 4-bit Mode: Data Line Bit [2] or Read Wait (optional) SDIO 1-bit Mode: Read Wait (optional) SDIO SPI Mode: Reserved	VDD_SHI
42	SDIO_D1	I/O	G-SPI mode : G-SPI Data Output SDIO/SPI Mode: SDIO 4-bit Mode: Data Line Bit [1] SDIO 1-bit Mode: Interrupt SDIO SPI Mode: Reserved	VDD_SHI
43	SDIO_D0	I/O	G-SPI Mode: G-SPI Chip Select Input (active low) SDIO 4-bit Mode: Data Line Bit [0] SDIO 1-bit Mode: Data line SDIO SPI Mode: Data output	VDD_SHI
44	SDIO_CMD	I/O	G-SPI mode : G-SPI Data Input SDIO 4-bit Mode: Command/Response SDIO 1-bit Mode: Command Line SDIO SPI Mode: Data Input	VDD_SHI
45	SDIO_CLK	I	G-SPI Mode: G-SPI Clock Input SDIO 4-bit Mode: Clock Input SDIO 1-bit Mode: Clock Input SDIO SPI Mode: Clock Input	VDD_SHI
46	GND	Ground	Ground	Ground
47	VDD1.8	Power	1.8V Power supply for baseband and internal LDO	VDD1.8
48	GND	Ground	Ground	Ground

6.2 SPECIFICATIONS AND TIMING DIAGRAM

6.2.1 INPUT CLOCK

19.2MHz Clock Timing

NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
T _{P_XO19_2}	XO19_2 period	--	52.083 - 20 ppm	52.083	52.083 + 20 ppm	ns
T _{H_XO19_2}	XO19_2 high time	--	20.8332	26.0415	31.2498	ns
T _{L_XO19_2}	XO19_2 low time	--	20.8332	26.0415	31.2498	ns
T _{R_XO19_2}	XO19_2 rise time	--	--	--	5	ns
T _{F_XO19_2}	XO19_2 fall time	--	--	--	5	ns

20MHz Clock Timing

NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
T _{P_XO20}	XO20 period	--	50.000 - 20 ppm	50.000	50.000 + 20 ppm	ns
T _{H_XO20}	XO20 high time	--	20.000	25.000	30.000	ns
T _{L_XO20}	XO20 low time	--	20.000	25.000	30.000	ns
T _{R_XO20}	XO20 rise time	--	--	--	5	ns
T _{F_XO20}	XO20 fall time	--	--	--	5	ns

26MHz Clock Timing

NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
T _{P_XO26}	XO26 period	--	38.462 - 20 ppm	38.462	38.462 + 20 ppm	ns
T _{H_XO26}	XO26 high time	--	15.3848	19.231	23.0772	ns
T _{L_XO26}	XO26 low time	--	15.3848	19.231	23.0772	ns
T _{R_XO26}	XO26 rise time	--	--	--	5	ns
T _{F_XO26}	XO26 fall time	--	--	--	5	ns

38.4MHz Clock Timing

Description Product Specification – WM-G-MR-05

NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
T _{P_XO38_4}	XO38_4 period	--	26.042 - 20 ppm	26.042	26.042 + 20 ppm	ns
T _{H_XO38_4}	XO38_4 high time	--	10.4168	13.021	15.6252	ns
T _{L_XO38_4}	XO38_4 low time	--	10.4168	13.021	15.6252	ns
T _{R_XO38_4}	XO38_4 rise time	--	--	--	5	ns
T _{F_XO38_4}	XO38_4 fall time	--	--	--	5	ns

40MHz Clock Timing

NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
T _{P_XO40}	XO40 period	--	25.000 - 20 ppm	25.000	25.000 + 20 ppm	ns
T _{H_XO40}	XO40 high time	--	10.000	12.500	15.000	ns
T _{L_XO40}	XO40 low time	--	10.000	12.500	15.000	ns
T _{R_XO40}	XO40 rise time	--	--	--	5	ns
T _{F_XO40}	XO40 fall time	--	--	--	5	ns

6.2.2 EXTERNAL SLEEP CLOCK SPECIFICATION

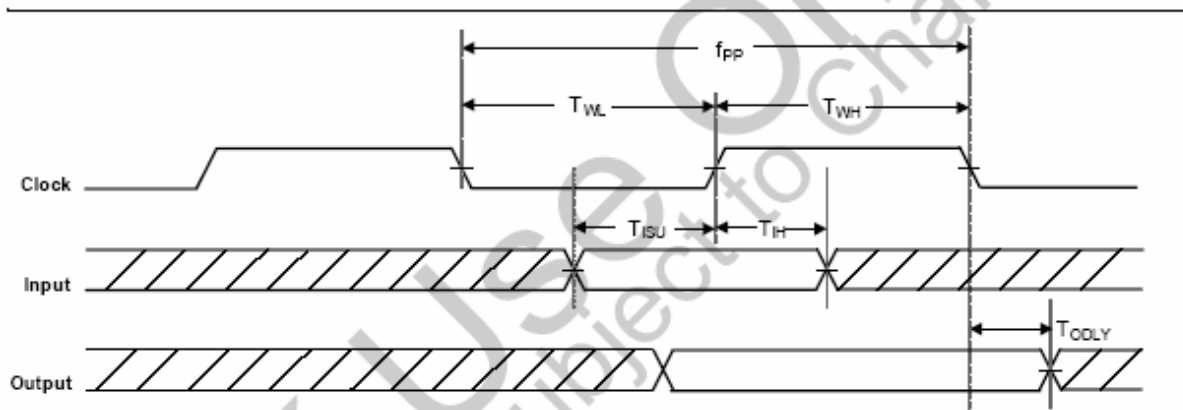
The WM-G-MR-05 external sleep clock pin (SLEEP_CLK) is powered from VDD_SHI Voltage Supply

Protocol Timing

NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
CLK	Clock Frequency Range	--	10	100	1000	kHz
T _{HIGH}	--	--	40	--	--	ns
T _{LOW}	--	--	40	--	--	ns
T _{RISE}	--	--	--	--	5	ns
T _{FALL}	--	--	--	--	5	ns

6.2.3 SDIO PROTOCOL TIMING



Note

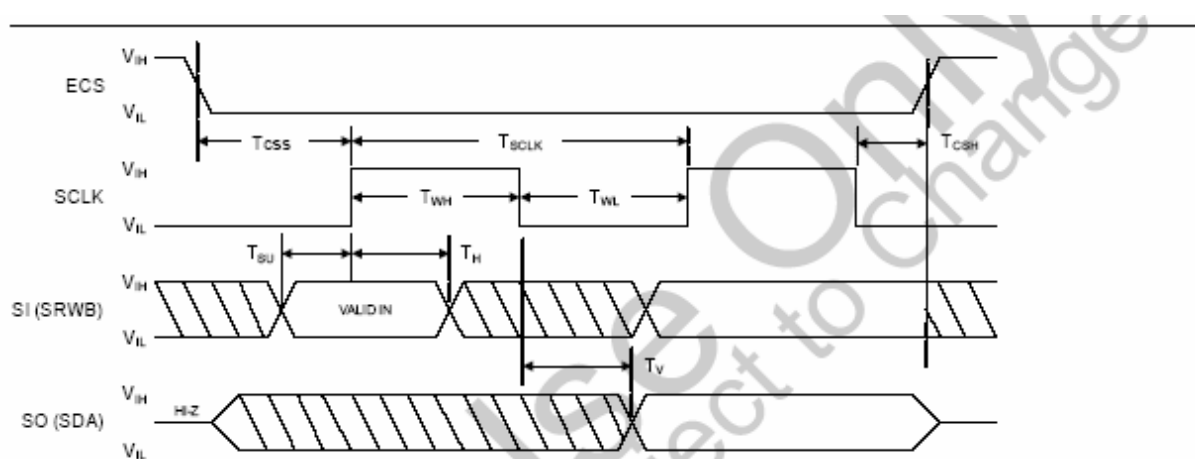
The SDIO-SPI CS signal timing is identical to all other SDIO inputs.

SDIO Timing Data

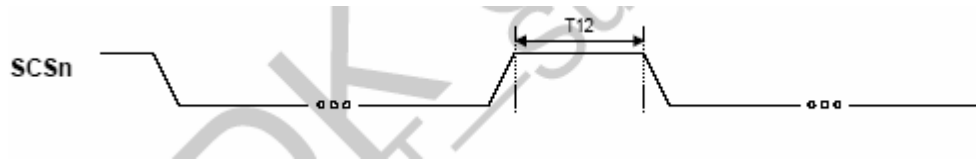
NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	CLK Frequency	--	0	--	45	MHz
T_{WL}	CLK Low Time	--	11.1	--	--	ns
T_{WH}	CLK High Time	--	11.1	--	--	ns
T_{ISU}	Input Setup Time	--	5	--	--	ns
T_{IH}	Input Hold Time	--	5	--	--	ns
T_{ODLY}	Output Delay Time	--	0	--	15	ns

6.2.4 SPI PROTOCOL TIMING



G-SPI Interface Inter Transaction Timing



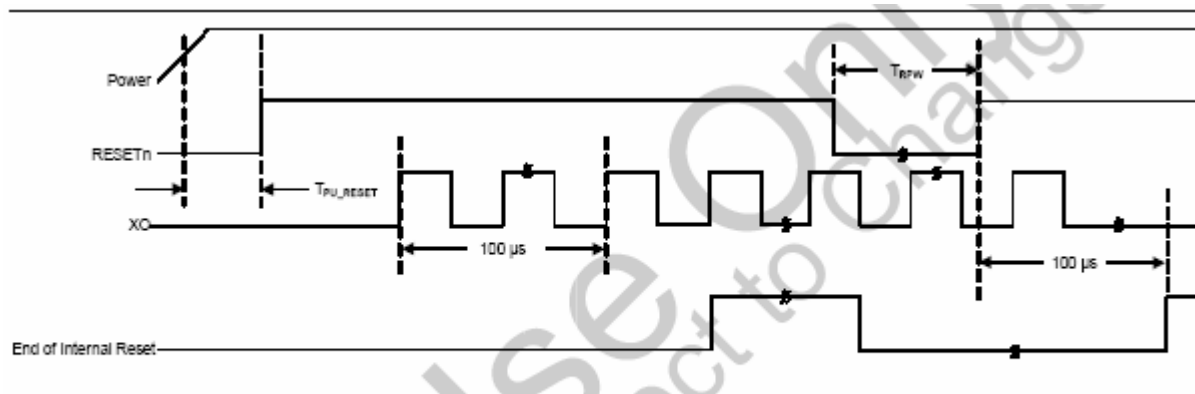
SPI Interface Timing Data

NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Units
T1	Clock Period	20	--	--	ns
T2	Clock High	5	--	--	ns
T3	Clock Low	9	--	--	ns
T4	Clock Rise Time	--	--	1	ns
T5	Clock Fall Time	--	--	1	ns
T6	SDI Hold Time	2.5	--	--	ns
T7	SDI Setup Time	2.5	--	--	ns
T8	SDO Hold Time	5	--	--	ns
T9	SDO Setup Time	1	--	--	ns
T10	SCSn Fall to Clock	5	--	--	ns
T11	Clock to SCSn Rise	0	--	--	ns
T12	SCSn Rise to SCSn Fall	400	--	--	ns

6.2.5 CO-EXISTANCE PROTOCOL TIMING
TBD

6.2.6 RESET AND CONFIGURATION TIMING



Notes

- RESETn is not needed for proper operation due to internal power-on reset logic.

RESETn Timing Requirement.

NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{PU_RESET}	Valid power to RESETn de-asserted	--	0	--	--	ms
T_{RPW}	RESETn pulse width	--	10^1	100	--	ns

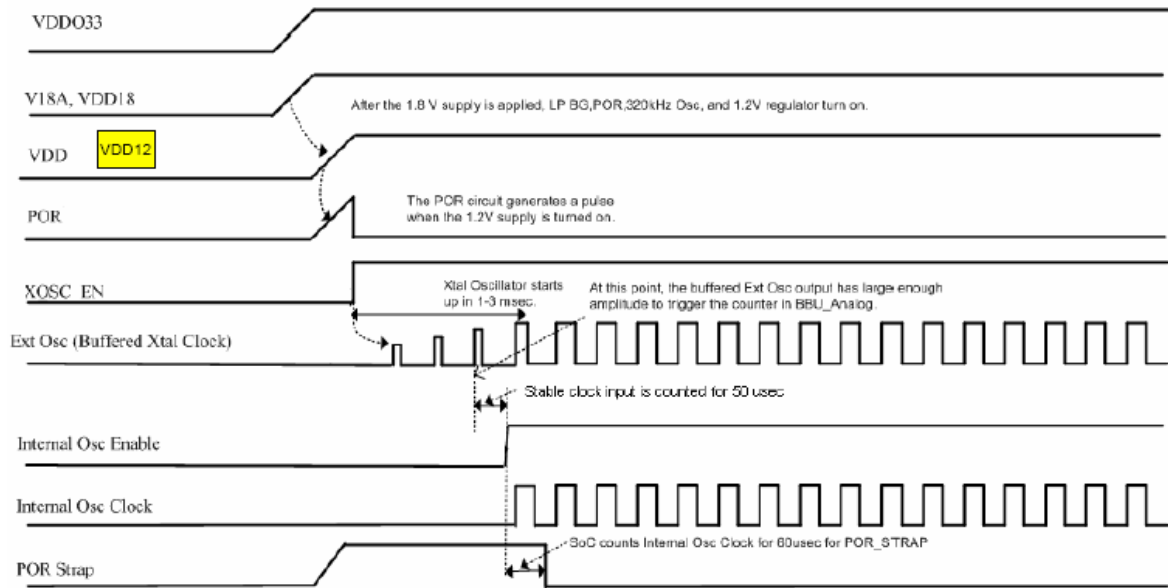
1. This is the minimum value guaranteed for a valid reset. Smaller values may trigger the reset circuit.

Internal Reset Timing

NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

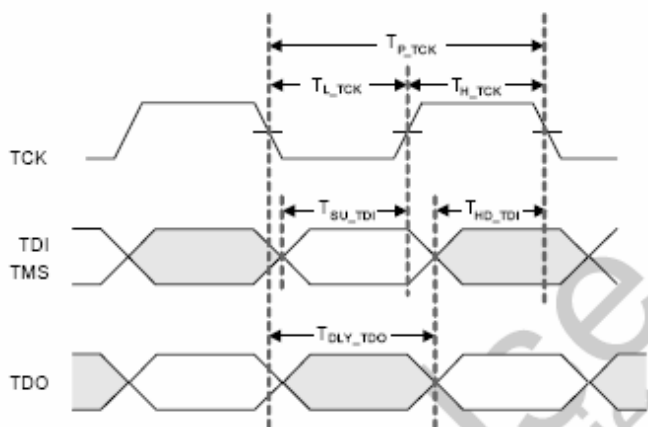
Symbol	Parameter	Condition	Min	Typ	Max	Units
--	Negative internal reset pulse width	--	100	100	--	μs

6.2.7 POWER UP SEQUENCE



- VDD18 feeds the internal 1.2V regulator (VDD)
- VDD18 must be completely stabilized by 60 us after clock reference stabilizes

6.2.8 JTAG SPECIFICATION



JTAG TIMING

Description Product Specification – WM-G-MR-05

NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
T _{P_TCK}	TCK Period	--	40	--	--	ns
T _{H_TCK}	TCK High	--	12	--	--	ns
T _{L_TCK}	TCK Low	--	12	--	--	ns
T _{SU_TDI}	TDI, TMS to TCK Setup Time	--	10	--	--	ns
T _{HD_TDI}	TDI, TMS to TCK Hold Time	--	10	--	--	ns
T _{DLY_TDO}	TCK to TDO Delay	--	0	--	15	ns



Note

Does not apply to CPU JTAG enabled by the TMS_SYS pins.

6.2.9 LED INTERFACE

Pin No.	Pin description	Function description
14	WLAN_LED	Check firmware specification of GPIO(1) with Marvell

NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Typ	Units
I _{OH}	Switching current high	Tristate on pad (requires pull-up on board)	Tristate when driving high	mA
I _{OL}	Switching current low	@ 0.4V	10	mA

1. LED Mode is independently selectable for the GPIO[1].

6.2.10 ANTENNA INTERFACE

Antenna diversity is not supported on the Wireless Module.
The output impedance of the antenna port is 50 Ohms.

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7 REGULATORY

The WM-G-MR-05 module is pre-tested on module level to comply with following standards (pre-test):

- US/CAN: FCC CFR47 Part 15.247
- Europe: ETS 300-328 V1.6.1
- Japan : TELEC

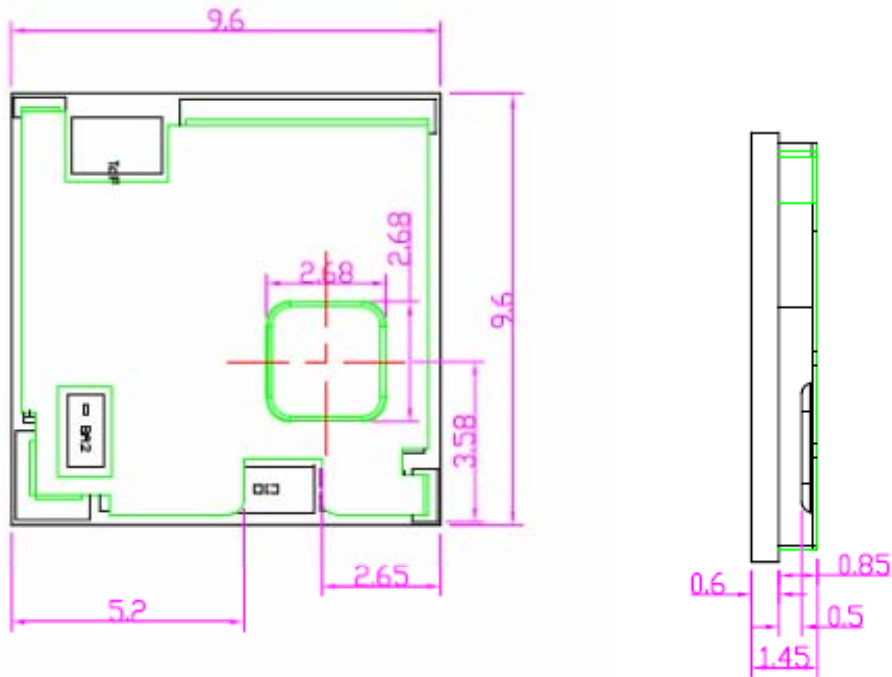
Test setup: laptop plus adaptor card with Marvell Labtool in SDIO mode

Final certification should be completed on system level.

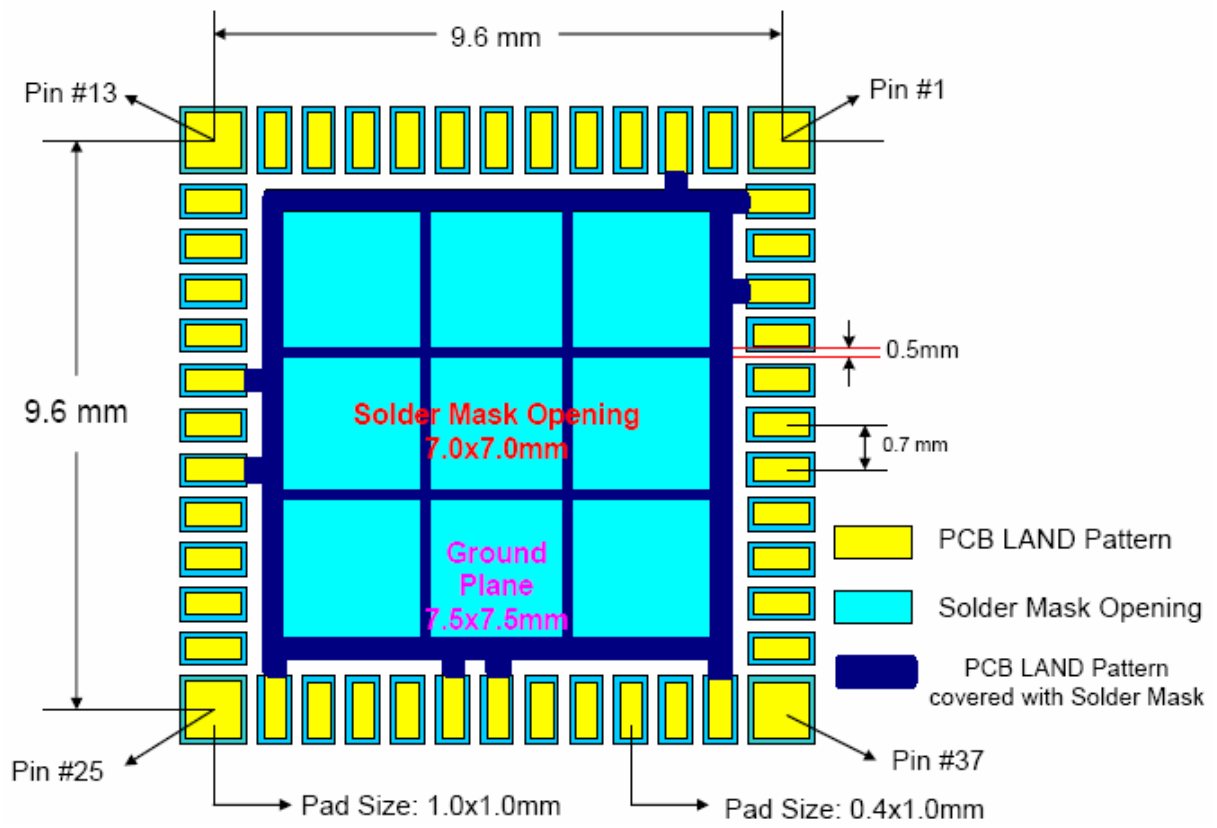
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8 MECHANICAL SPECIFICATION

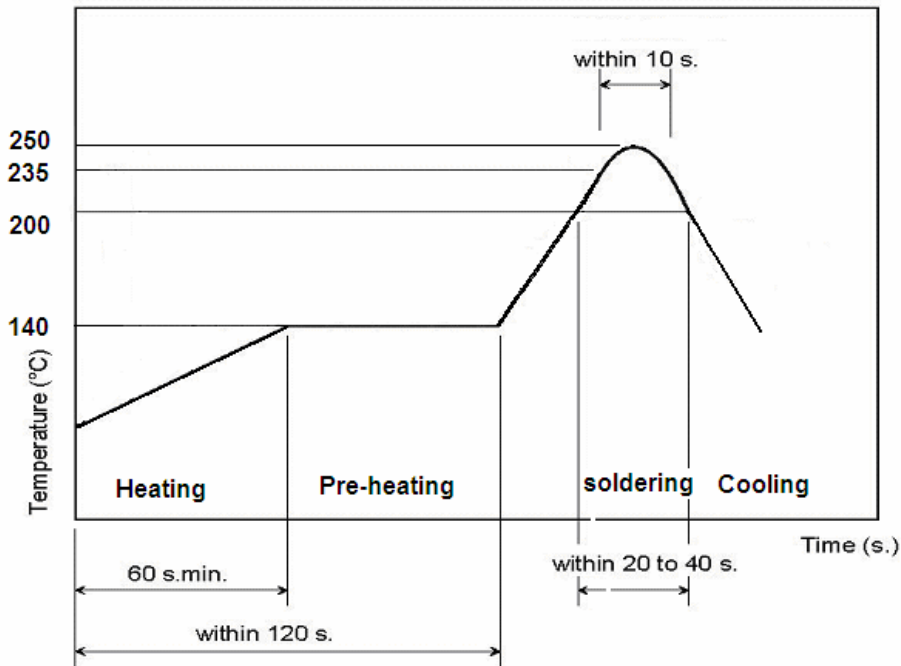
Dimension : 9.6x9.6x1.45 mm



9 RECOMMENDED FOOTPRINT



10 RECOMMENDED REFLOW PROFILE



11 PACKAGE AND STORAGE CONDITION

11.1 Package Dimension



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11.2 ESD Level

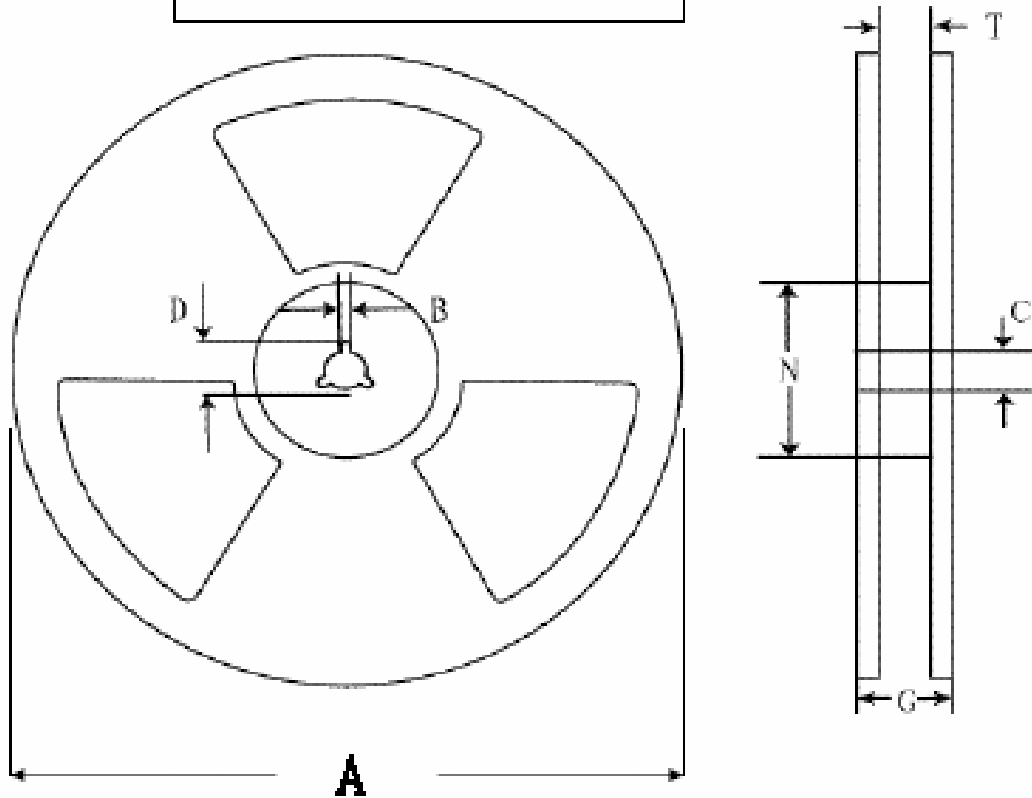
Note:

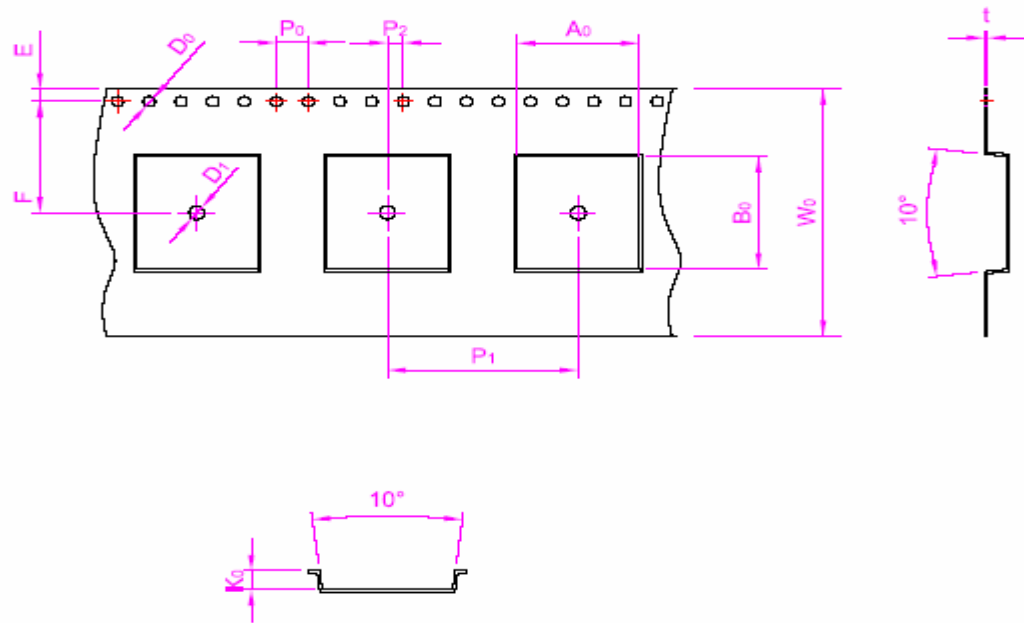
1. Surface Resistivity:
Interior: $10^9 \sim 10^{11} \Omega/\text{SQUARE}$
EXTERIOR: $10^8 \sim 10^{12} \Omega/\text{SQUARE}$
2. Dimension: 475*420mm
3. Tolerance: +5,0mm
4. Color:
Background : Gray
Text : Red

11.3 Tap/Reel Dimension

Embossed carrier tape	Top cover tape	Each Item Size						
		W \pm 0.15m/m	W \pm 0.15m/m	A	B \pm 0.5	D \pm 1.0	C \pm 0.2	N \pm 1.0
8	5.3/5.5	330	2.2	20.2	13	100	8.5	13.1
12	9.3	330	2.2	20.2	13	100	12.5	17.1
16	13.3	330	2.2	20.2	13	100	16.5	21.1
24	21.3	330	2.2	20.2	13	100	24.5	29.1
32	25.5	330	2.2	20.2	13	100	32.5	37.1
44	37.5	330	2.2	20.2	13	100	44.5	49.1
56	49.5	330	2.2	20.2	13	100	56.5	61.1

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ITEM	A_0	B_0	D_0	D_1	E	F	K_0
SPEC	9.9 ± 0.1	9.9 ± 0.1	$1.50 + 0.1 / -0$	$1.5 + 0.1 / -0$	1.75 ± 0.1	11.5 ± 0.1	1.95 ± 0.1
ITEM	K_1	P_0	P_1	P_2	$P_0 \times 10$	t	W_0
SPEC		4.00 ± 0.1	12.0 ± 0.1	2.00 ± 0.1	Cumulative Tolerance ± 0.2	0.40 ± 0.05	24 ± 0.3

Length leader / trailer tape:

Leader tape: ≥ 550 mm which includes ≥ 100 mm of carrier tape with empty compartments and covered with tape; remaining part might be of cover tape only.

Trailer tape: ≥ 160 mm with empty compartments and covered with tape.

NOTES:

1. Material: Conductive Polystyrene (Recycle)

2. Color: Black

3. Surface resistance: 10^6 Ohms/square 以下

3. Cumulative tolerance per 10 pitches (P_0) is ± 0.2 mm.

4. Carrier camber shall be not more than 1mm per 100mm, noncumulative over 250mm

5. A_0 & B_0 are measured on the plane by 0.3 mm above the bottom of the pocket.

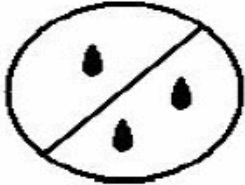
6. K_0 is measured from the inside bottom of the pocket to the top surface of the carrier.

7. Pocket position relative to sprocket hold is measured as true position of pocket, not sprocket hold.

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Description Product Specification – WM-G-MR-05

11.4 MSL Level / Storage Condition

	<p>CAUTION This bag contains MOISTURE-SENSITIVE DEVICES</p>	<p>LEVEL</p> <div style="border: 2px solid black; padding: 10px; width: 60px; margin: 0 auto;"> <p style="font-size: 24px; margin: 0;">4</p> </div> <p style="font-size: 8px; margin: 0;">If Blank, see adjacent bar code label</p>
<p>1. Calculated Shelf life in sealed bag: 12 months at < 40°C and < 90%Relative humidity (RH)</p> <p>2. Peak package body temperature <u>240</u> °C <small>If Blank, see adjacent bar code label</small></p> <p>3. After bag is opened, Devices that will be subjected to reflow solder or other high temperature process must</p> <p>(a) Mounted within: <u>72</u> hrs. Of factory conditions ≤ 30°C/60% RH, OR <small>If Blank, see adjacent bar code label</small></p> <p>(b) Stored at < 10°C RH.</p> <p>4. Devices require bake, before mounting, it:</p> <p>(a) Humidity indicator Card is >10% when read at 23±5°C</p> <p>(b) 3a or 3b not met.</p> <p>5. If baking is required, Devices may be baked for 24 hrs at 125±5°C</p> <p>Note: If device containers cannot be subjected to high temperature Or shorter bake times are desired. Reference IPC/JEDEC J-STD-033 for bake procedure</p> <p>Bag Seal Date: _____ Note: Level and body temperature defined by IPC/JEDEC J-STD-020 <small>If Blank, see adjacent bar code label</small></p>		